艾碧科技股份有限公司
abietec Inc.

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Approval Sheet

(產品承認書)

產品名稱	(Product)	Wi-Fi and BLE Combo Module
解決方案	(Solution)	Infineon CYW55912 WLBGA Package
產品型號	(Model No.)	**AI55912-P** (PCB Antenna)

Index

1. Overall introduction

abietec's AI55912 is a Wi-Fi and BLE combo module designed based on **Infineon CYW55912 MCU solution**, which incorporates: **GPIO**, **QSPI, SPI**, **SDIO, UART**, **I2C**, **I2S, PDM, TDM, PWM, and ADC** interfaces for connecting peripherals.

Features:

1. Integrates a 192 MHz Arm® Cortex® M33 processor embedded in the 2048 KB of ROM.
2. Dual Transmission mode of BLE & Wi-Fi dual bands RF , according to the customer's preference.
3. Compact size with **(L) 22.0 x (W) 13.6 x (H) 2.3mm**
4. Supports dual bands, single stream, 1x1, Wi-Fi 6 (802.11ax) over 20MHz channels.
5. Supports Bluetooth® LE 5.4 with support for LE 1 Mbps, LE 2 Mbps, and LE long range.
6. Fully integrated with RF antenna and shielding
7. Operates over the -40°C to +85°C temperature range.

1.1. Specification

- Connected MCU
  - Arm® Cortex®-M33 192 MHz - On-chip memory has
    - 2048-KB ROM
    - 768-KB RAM
    - 1 x Serial memory interface (SMIF)
  - **Supports interface with other Host MCUs for Network Offloads and Network communication over AT Commands interface**
    - > 40 Mbps throughput with TCP/IP, TLS over SDIO
    - > 20 Mbps throughput with TCP/IP, TLS over gSPI
    - > 7.4 Mbps throughput with TCP/IP, TLS over UART
- **Wide selection of peripherals**
  - **3 x Serial Communication Blocks configurable as SPI, I2C or UART**
    - UART (< 7.4 Mbps)
    - I2C (100 kHz, 400 kHz, and 1 MHz)
    - SPI (< 24 MHz)
  - **9 x Timer Counter PWM (TCPWM)**
    - 2 x 32-bit + 7 x 16-bit counters, 4 x OUT positive/negative, 8 x IN
  - **1 x PDM (Digital microphone)**
  - **2 x TDM**

- **Audio Interfaces**
  - TDM1, TDM2 each supporting inter-IC sound (I2S) (2-channels) and PCM (8-channels), 8k to 96k sample rates, and 16- and 24-bit sample widths
  - Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates and 16-bit sample width. Multiplexed with TDM2 through the second audio interface
  - Single-direction I2S with 48k sample rates and 16-bit sample width. Multiplexed with TDM2 through the second audio interface
- **GPIO**
  - Up to 47 GPIOs
- **Timer/Watchdog**
  - 2x Timer
  - 1x Watchdog
- **Programming and debugging**
  - Debug Supported via ARM DAP JTAG/SWD
  - Programming supported via UART

- **WLAN features**
  - IEEE 802.11a/b/g/n/ac/ax compliant
  - Dual-band (2.4 GHz/5 GHz)
  - 1x1 with 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
  - Transmit (TX) power with internal PA
    - 2.4 GHz: +24 dBm 1Mbps DSSS
    - 5 GHz: +20.5 dBm 6Mbps OFDM
  - Sensitivity with internal LNA
    - 2.4 GHz: -101.5 dBm 1Mbps DSSS
    - 5 GHz: -94.5 dBm MCS0
  - Wi-Fi 6 release features
    - OFDMA uplink and downlink as STA
    - Downlink multi-user MIMO (MU-MIMO) as STA
    - Individual target-wake-time (TWT), broadcast TWT
    - BSS color
  - Security
    - WPA2(Personal/Enterprise), WPA3 (Personal/Enterprise with 192-bit security)

- **Bluetooth® Low Energy**

  - Bluetooth® 5.4 (Bluetooth® Low Energy)
    - Advertising Coding Selection
    - Encrypted Advertising Data
    - LE Generic Attribute Profile (GATT) Security Levels Characteristic
  - Bluetooth® Low Energy 5.0/5.1/5.2/5.3 features
    - Advertisement Data Information (ADI) in Periodic Advertising
    - LE Enhanced Connection Update
    - LE Channel Classification
    - LE Isochronous Channels (non-Audio applications)
    - Enhanced Attribute Protocol
    - LE Power Control
    - GATT caching
    - Periodic Advertising Sync Transfer (PAST)
    - Control Length Extension
    - Advertising Channel Index
    - Slot Availability Mask (SAM)
    - 2M PHY for LE
    - LE Coded PHY
    - High Duty Cycle Non-Connectable Advertising
    - LE Advertising Extensions
    - LE Channel Selection Algorithm #2
  - Bluetooth® LNA can be shared with WLAN LNA for reduced antenna count (sLNA)
  - Dedicated Bluetooth® LNA (dLNA) for improved RF and coexistence performance with dedicated Bluetooth® antenna
  - +4, +13, and +19 dBm Bluetooth® PA paths optimized for best efficiency, output power adjustable in 4 dB steps
  - Receive sensitivity: -111.5 dBm (Bluetooth® LE 125 kbps, LR S=8)
  - Receive sensitivity: -97.5 dBm (Bluetooth® LE 2 Mbps)
  - Bluetooth® UART with a max baud rate of 4 Mbps

- **General features**

  - VBAT: 3.3 V typical, 3.0 V to 4.8 V operating range
  - VDDIO: 1.8 V typical
  - Temperature range: –40°C to +85°C
  - External 32.768 kHz low-power oscillator (LPO) with crystal or reference clock input for low-power consumption

- **Security**

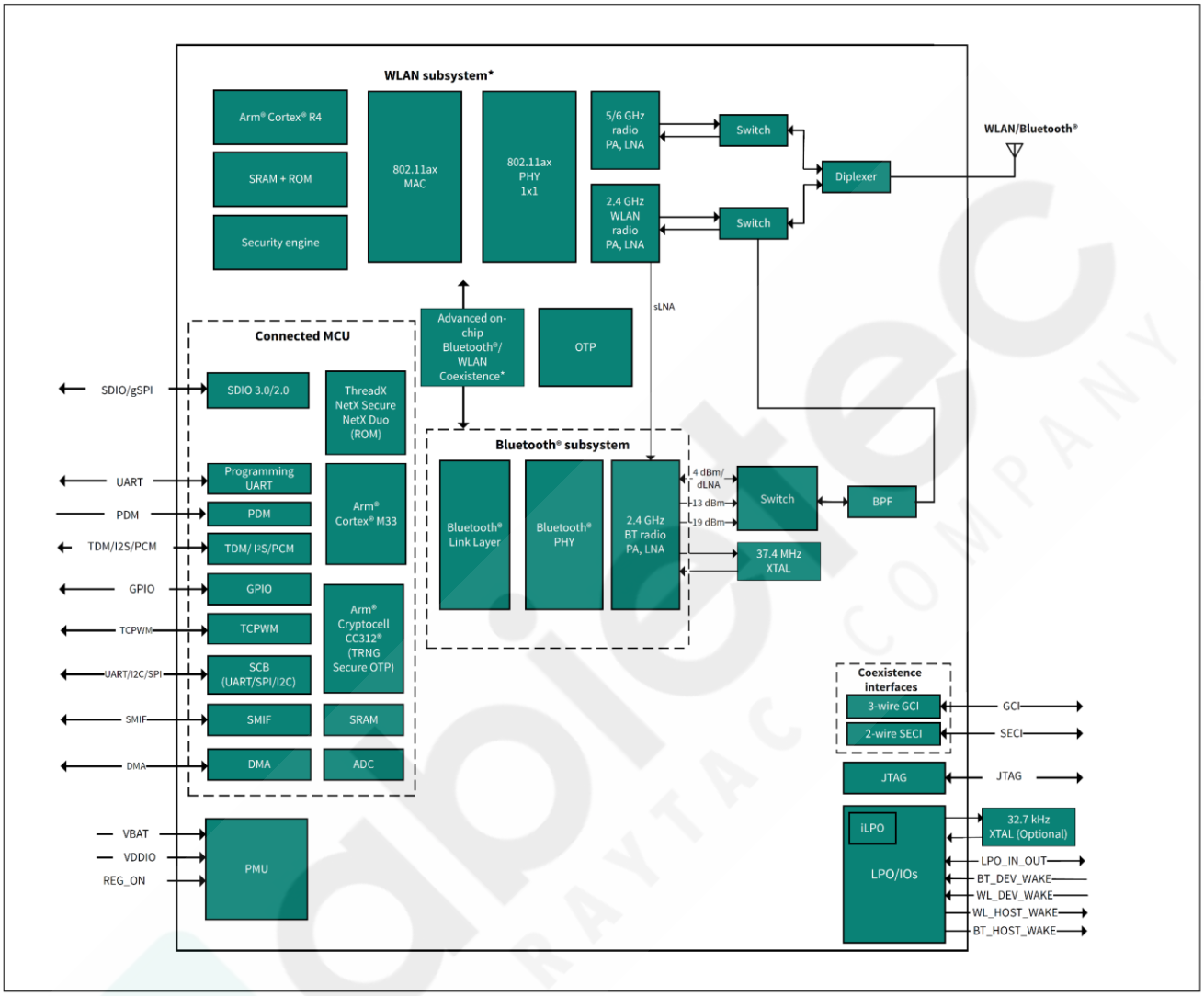
  - Arm® Trustzone Cryptocell 312
  - Wi-Fi, Bluetooth®, and application-independent firmware authentication
  - Firmware encryption

1.2. Potential applications

-IP Cameras
-Video Doorbell Cameras
-Smart Locks
-Smart Watches
-IoT Gateways
-Sensors
-Wi-Fi Speakers
-Thermostats
-Appliances
-Printers
-Internet of Things (IoT)
-Industrial Internet of Things (IIoT)
-Smart Home
-Boilers
-Garage Door Openers (GDO)

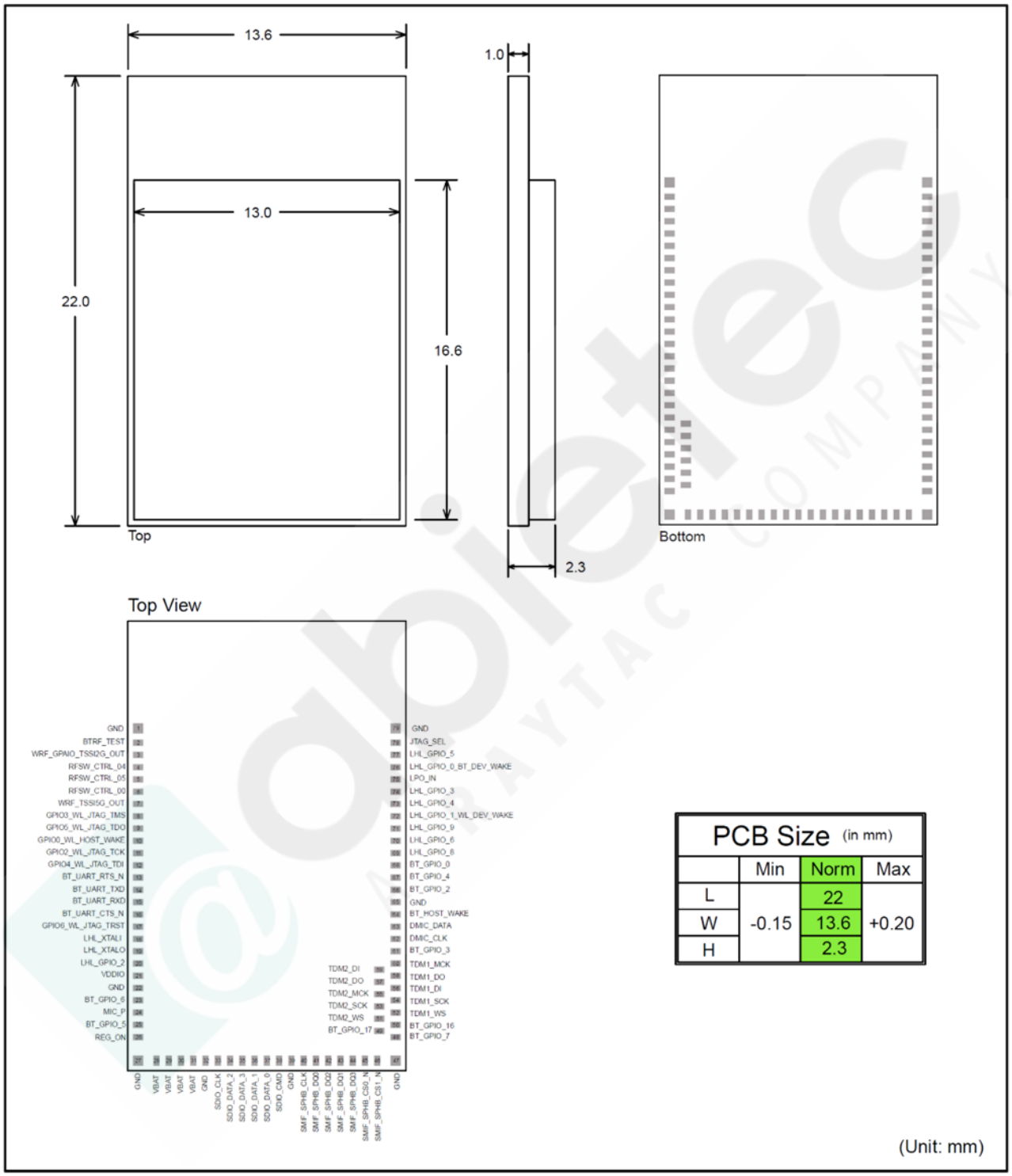
2. Product dimension

2.1. Block diagram



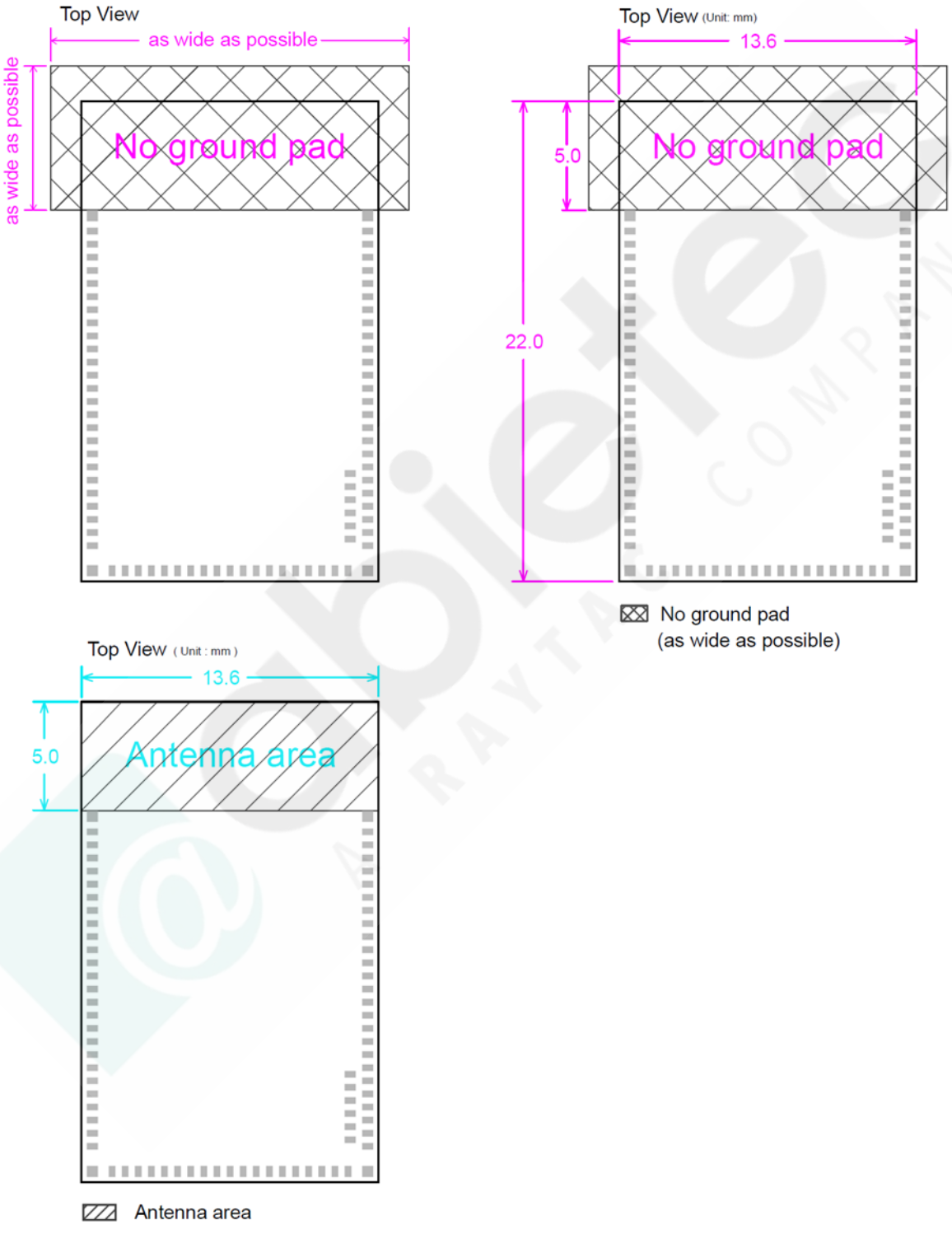
2.2. PCB dimensions & pin Indication

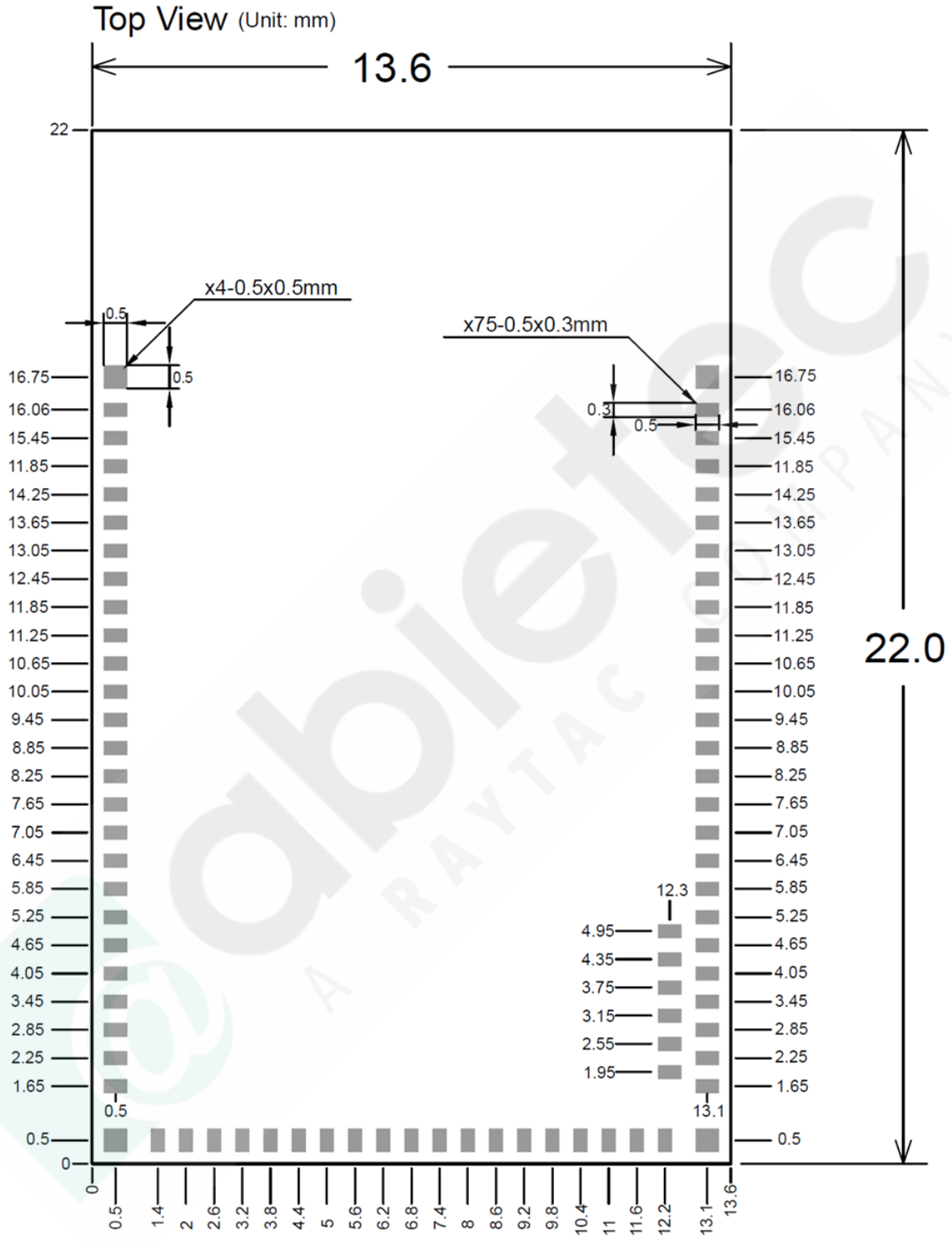
- **AI55912-P**



2.3. Recommended layout of solder pad

Graphs are all in Top View, Units in mm.

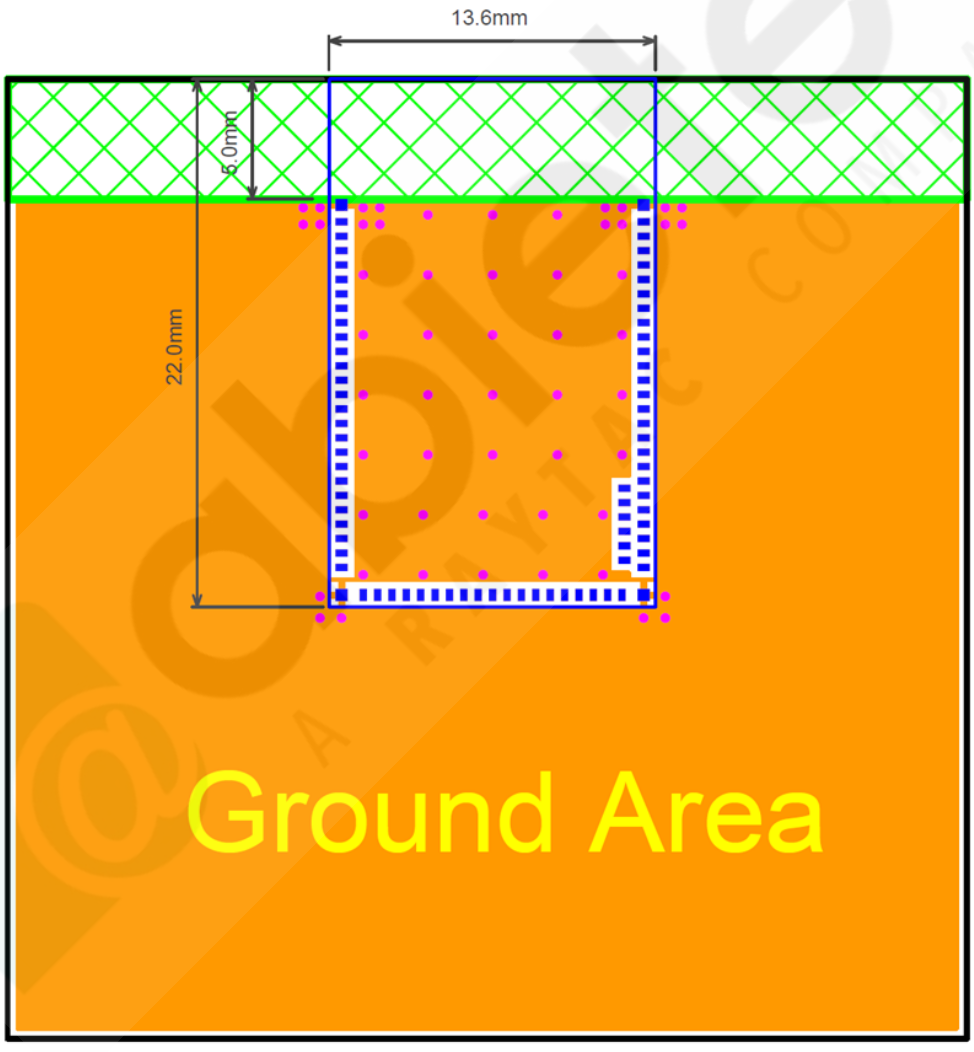



Top View (Unit: mm)
13.6
22
22.0
x4-0.5x0.5mm
x75-0.5x0.3mm
0.5
0.3
16.75
16.06
15.45
11.85
14.25
13.65
13.05
12.45
11.85
11.25
10.65
10.05
9.45
8.85
8.25
7.65
7.05
6.45
5.85
5.25
4.65
4.05
3.45
2.85
2.25
1.65
0.5
0
12.3
4.95
4.35
3.75
3.15
2.55
1.95
13.1
0
0.5
1.4
2
2.6
3.2
3.8
4.4
5
5.6
6.2
6.8
7.4
8
8.6
9.2
9.8
10.4
11
11.6
12.2
13.1
13.6

2.4. RF layout suggestion (AKA, antenna keep-out area)

Please ensure that no ground pad overlaps the “No Ground-Pad Area”, as shown in the images below. This is important to maintain antenna performance and to prevent potential short circuits within the module.

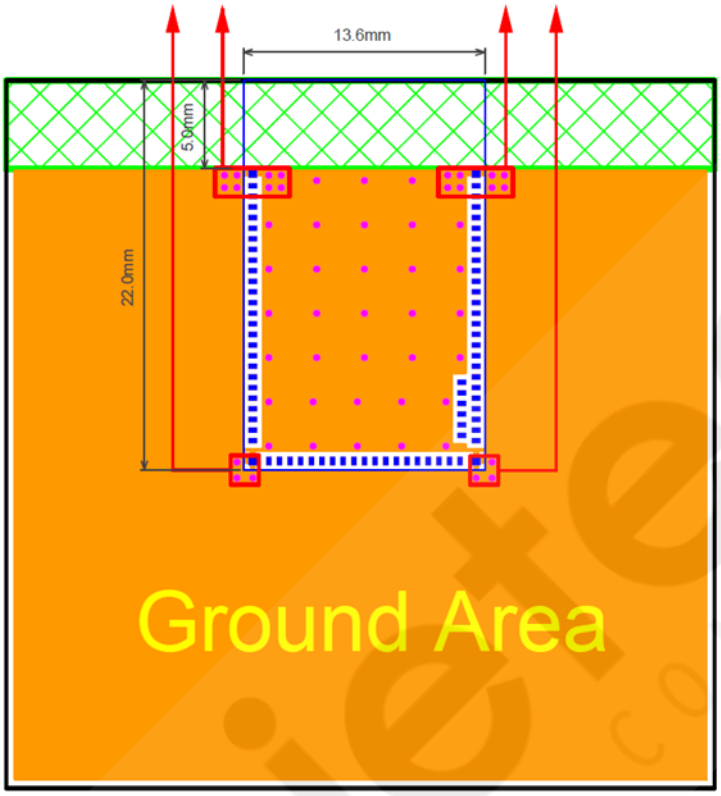
You are welcome to send us your design files for review at service@abietec.com or to your abietec contact with email subject titled: “Layout Review – **abietec** Model No. – Your company name”.



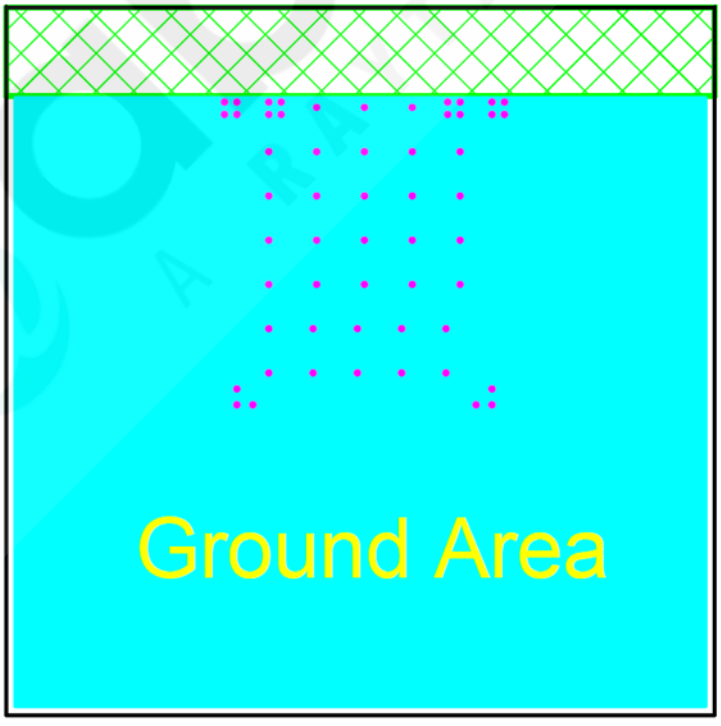
Top View

No Ground Pad Area

Please add via holes in GROUND area as many as possible, especially around the four corners.



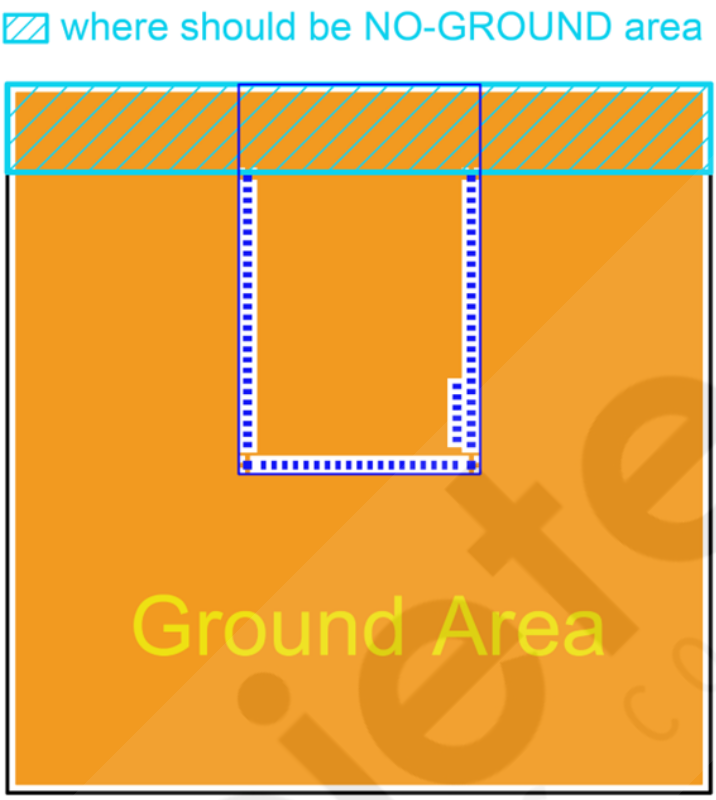
Top View

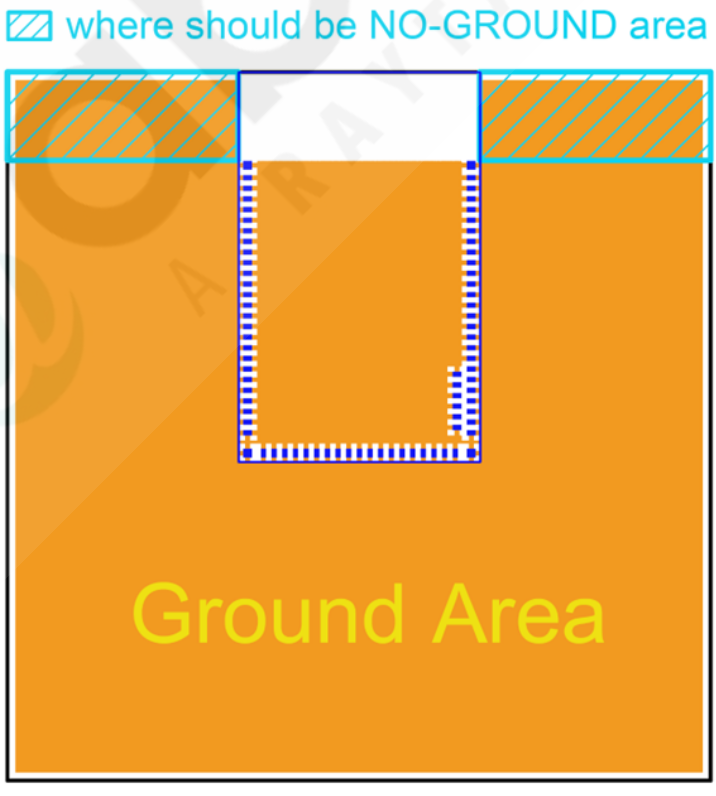


Perspective View

No Ground Pad Area

Examples of “**NOT RECOMMENDED**” layout





2.5. Pin assignment

Pin No.	Name	Pin function	Description
(1)(22) (27)(32) (39)(47) (65)(79)	GND	Ground	The pad must be connected to a solid ground plane
(2)	BTRF_TEST	I/O	Bluetooth® Radio test input/output
(3)	WRF_GPAIO_TSSI2G_OUT	O	WLAN Radio 2.4 GHz TSSI
(4)	RFSW_CTRL_04	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
(5)	RFSW_CTRL_05		
(6)	RFSW_CTRL_00		
(7)	WRF_TSSI5G_OUT	O	WLAN Radio 5/6 GHz TSSI
(8)	GPIO3_WL_JTAG_TMS	I/O	WLAN general-purpose I/O
(9)	GPIO5_WL_JTAG_TDO		
(10)	GPIO0_WL_HOST_WAKE		
(11)	GPIO2_WL_JTAG_TCK		
(12)	GPIO4_WL_JTAG_TDI		
(17)	GPIO6_WL_JTAG_TRST		
(13)	BT_UART_RTS_N	O	UART request-to-send. Active low request-to-send Signal for the BT UART interface. Bluetooth® LED control pin.
(14)	BT_UART_TXD	O	UART serial output. Serial data output for the BT UART interface.
(15)	BT_UART_RXD	I	UART serial input. Serial data input for the BT UART interface.
(16)	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the BT UART interface.
(18)	LHL_XTALI	I	32.768 kHz crystal oscillator input
(19)	LHL_XTALO	O	32.768 kHz crystal oscillator output
(20)	LHL_GPIO_2	I/O	Miscellaneous general-purpose I/O
(74)	LHL_GPIO_3		
(73)	LHL_GPIO_4		
(77)	LHL_GPIO_5		

Pin No.	Name	Pin function	Description
(70)	LHL_GPIO_6	I/O	Miscellaneous general-purpose I/O
(69)	LHL_GPIO_8		
(71)	LHL_GPIO_9		
(21)	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
(23)	BT_GPIO_6	I/O	Bluetooth® general-purpose I/O
(25)	BT_GPIO_5		
(48)	BT_GPIO_7		
(49)	BT_GPIO_17		
(50)	BT_GPIO_16		
(61)	BT_GPIO_3		
(66)	BT_GPIO_2		
(67)	BT_GPIO_4		
(68)	BT_GPIO_0		
(24)	MIC_P	I	ADC microphone positive input
(26)	REG_ON	I	Used by the PMU to power up or power down the internal CYW5591x regulators . When deasserted, this pin holds the chip in reset. This pin has an internal 50 kΩ pull-down resistor that is auto-enabled and disabled upon recognizing a high on this pin.
(28)(29)	VBAT	PWR	Battery supply input for ASR power stage
(33)	SDIO_CLK	I	SDIO clock input
(34)	SDIO_DATA_2	I/O	SDIO data line 2
(35)	SDIO_DATA_3		SDIO data line 3
(36)	SDIO_DATA_1		SDIO data line 1
(37)	SDIO_DATA_0		SDIO data line 0
(38)	SDIO_CMD		SDIO command line
(40)	SMIF_SPHB_CLK	O	SMIF clock output
(41)	SMIF_SPHB_DQ0	I/O	SMIF data line 0
(42)	SMIF_SPHB_DQ2		SMIF data line 2
(43)	SMIF_SPHB_DQ1		SMIF data line 1
(44)	SMIF_SPHB_DQ3	I/O	SMIF data line 3

Pin No.	Name	Pin function	Description
(45)	SMIF_SPHB_CS0_N	O	SMIF chip select0 active-low output
(46)	SMIF_SPHB_CS1_N		SMIF chip select1 active-low output
(51)	TDM2_WS	I/O	TDM2 Interface Word Select
(52)	TDM1_WS		TDM1 Interface Word Select
(53)	TDM2_SCK		TDM2 Interface Slave Clock
(54)	TDM1_SCK		TDM1 Interface Slave Clock
(55)	TDM2_MCK		TDM2 Interface Master Clock
(56)	TDM1_DI		TDM1 Interface Data In
(57)	TDM2_DO		TDM2 Interface Data Out
(58)	TDM1_DO		Bluetooth® TDM1 Interface Data Out
(59)	TDM2_DI		TDM2 Interface Data In
(60)	TDM1_MCK		TDM1 Interface Master Clock
(62)	DMIC_CLK	I/O	Digital mic clock
(63)	DMIC_DATA		Digital mic data
(64)	BT_HOST_WAKE	I/O	Bluetooth® HOST WAKE
(72)	LHL_GPIO_1_WL_DEV_WAKE	I/O	WLAN DEVICE WAKE
(75)	LPO_IN	I/O	Based on the configuration, it can be either 1. As an external 32 KHz clock source input 2. As a 32 KHz clock output if XTAL is connected (XTAL_IN, XTAL_OUT). 3. LHL_GPIO_10 is similar to other LHL GPIOs
(76)	LHL_GPIO_0_BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
(78)	JTAG_SEL	I	JTAG select input: Pull high to choose the Tessent Test Access Port, and connect this pin to ground to enable ARM™ Debug Access Port.

3. Power supplies and power management

3.1. Power supply topology

A buck regulator, multiple LDO regulators, and a power management unit are integrated into CYW5591x. These blocks simplify power supply design for Bluetooth® and WLAN functions in embedded designs. CYW5591x only requires two power supplies, VBAT, and VDDIO, to be provided, with all additional voltages being generated by on-chip regulators. Control signal REG_ON is used to power up the regulators and take the device out of reset. The core Buck regulator ABUCK powers up when REG_ON is asserted. All regulators, Buck and LDO, are powered down when REG_ON is deasserted. CYW5591x allows for an extremely low power-consumption mode by completely shutting down the ABUCK regulator.

3.2. CYW5591x family PMU features

CYW5591x contains the following regulators:

- Analog switching regulator (400 mA)
- BTLDO (400 mA)
- PALDO (400 mA)
- RFLDO (100 mA)
- CLDO (100 mA)

See the Internal Regulator Electrical Specifications for more details

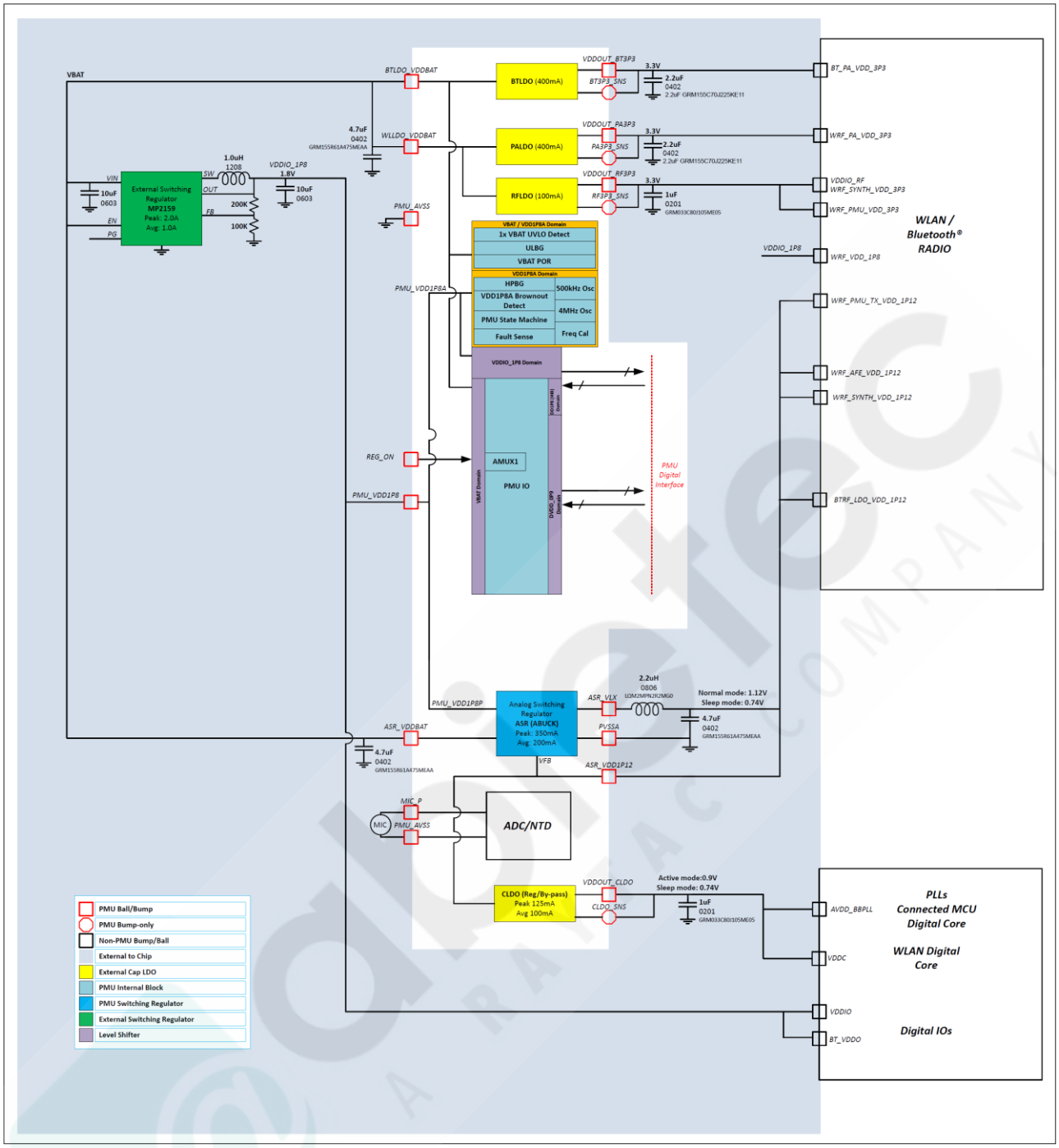


Figure 1 Typical power topology

3.3. WLAN power management

CYW5591x has been designed with the stringent performance requirements of commercial/consumer applications in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW5591x integrated RAM is a HIGH Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. CYW5591x includes an advanced WLAN PMU sequencer. The PMU

sequencer provides significant power savings by putting CYW5591x into various power management states appropriate to the current environment and activities that are being performed. The PMU enables and disables internal regulators, switches, and other blocks. CYW5591x WLAN power states are described as follows:

- **Active mode**: All WLAN blocks in CYW5591x are powered up and fully functional with active carrier sensing and frame transmission and reception. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Deep Sleep mode**: Most of the chip, including both analog and digital domains, and most of the regulators, are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to a minimum. In Deep Sleep mode, the primary source of power consumption is leakage current due to retention memory and flops.
- **Power-down mode**: CYW5591x is effectively powered OFF by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

3.4. PMU sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.
Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn ON/turn OFF individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

3.5. Power-off shutdown

CYW5591x provides a low-power shutdown feature that allows the device to be turned OFF while the host and any other devices in the system remain operational. When CYW5591x is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows CYW5591x to be effectively OFF while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.
During a low-power shut-down state, if VDDIO remains applied to CYW5591x, all outputs are tristated, and most input signals are disabled. The input voltages remain within the limits defined for regular operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables CYW5591x to be fully integrated in an embedded device and take full advantage of the lowest power-saving modes. When CYW5591x is

powered ON from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

3.6. Power-up/power-down/reset circuits

CYW5591x has two signals (see Table 1) that enable or disable Bluetooth® and WLAN circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see the MCU or Bluetooth® start-up timing diagram .

Table 1 Power-up/power-down/reset control signals

Signal	Description
REG_ON	This signal is used by the PMU to power up the device and to control the internal CYW5591x regulators. When this pin is HIGH, the regulators are enabled, and the core is out of reset. If REG_ON is LOW, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and can be disabled up on recognizing high on this pin.

3.7. Brownout (BOR) and UVLO

Post-POR release, the BOR and UVLO circuits monitor the voltages on the 1.8 V and VBAT supplies, respectively

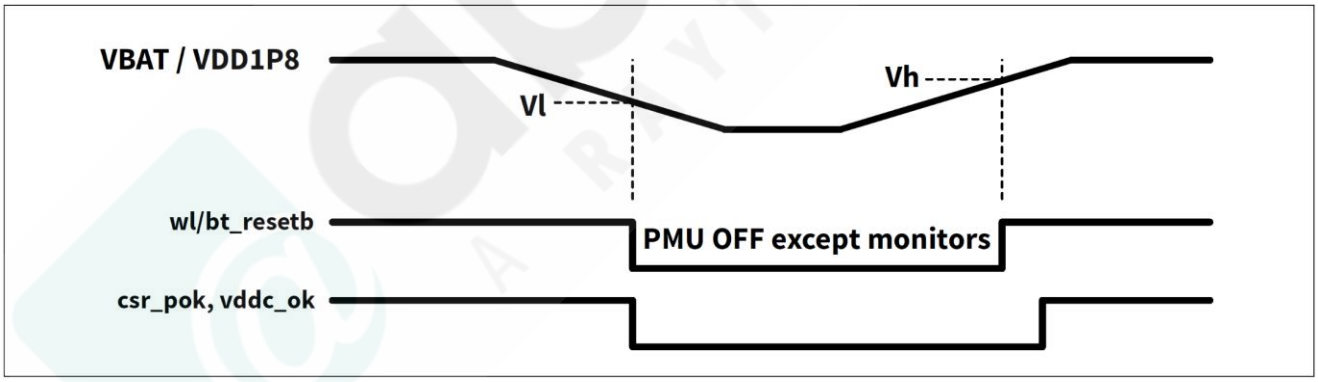


Figure 2 Brownout and UVLO

MCU or Bluetooth® start-up timing diagram

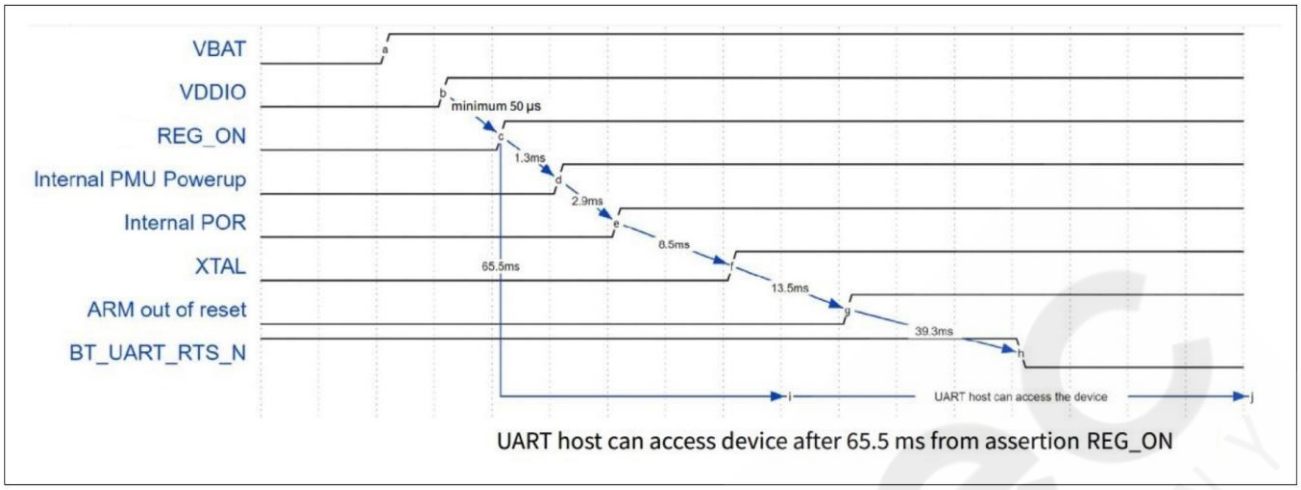


Figure 3 MCU/Bluetooth® subsystem start-up timing diagram

4. Internal regulator electrical specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

4.1. Main PMU

Table 2 PMU specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	–	3.0	3.3	4.8	V
I/O supply voltage	V_{DDIO}		1.71	1.80	1.89	
V_{BAT} UVLO threshold	V_{UVLO_RISE} V_{UVLO_FALL}	Rising (UVLO clear) Falling (UVLO set)	2.32 2.20	2.48 2.34	2.62 2.44	V
V_{DDIO} brownout threshold	V_{BRWO_RISE} V_{BRWO_FALL}	Rising (Brownout clear) Falling (Brownout set)	1.44 1.38	1.51 1.44	1.58 1.51	

5. Main chip solution

RF IC	Crystal Frequency
Infineon CYW55912 / WLBGA	**37.4MHz**

37.4MHz crystal is already inside the module.

6. Shipment packaging information

Model	Antenna	Photo
AI55912	Chip/Ceramic	
AI55912-P	PCB/Printed	
AI55912-U	U.FL/Connector	

6.1. Order code

Each model has two packaging options. Please use the following part number when placing an order with us.

Model	Tray
AI55912	WD-245C1-001
AI55912-P	WD-245C1-002
AI55912-U	WD-245C1-003

7. DC characteristics

Any technical spec shall refer to Infineon's official documents as the final reference. Contents below are from CYW55912-002 , please click to download the full spec.

7.1. Absolute maximum rating

Table 3 Absolute maximum ratings

Parameter	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 2.2	
Maximum undershoot voltage for I/O[1)]	Vundershoot	–0.5	
Maximum overshoot voltage for I/O[1)]	Vovershoot	VDDIO + 0.5	
Maximum input power for RX input ports[2)]	–	13	dBm

1) Duration not to exceed 25% of the duty cycle.
2) Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 13 dBm at a 1.5% duty-cycle derated from a 7-year lifetime.

7.2. Environmental ratings

Table 4 Environmental ratings

Characteristics	Value	Unit	Conditions
Ambient temperature (T_A)	–40 to +85	°C	Functional operation[1)]
Storage temperature	–40 to +125		–
Relative humidity	< 60	%	Storage
	< 85		Operation

1) The device is functional across this range of temperature. The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

7.3. Recommended operating conditions and DC characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 5, and operation outside these limits for extended periods can adversely affect the long-term reliability of the device.

Table 5 Recommended operating conditions and DC characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
DC supply voltage for VBAT	VBAT	3.0[1)]	3.3	4.8[2)]	V
DC supply voltage for digital I/O	VDDIO	1.71	1.8	1.89	
DC supply voltage for RF switch I/Os when supporting 3.3 V RF_SW_CTRL pads	VDDIO_RFSW	3.13	3.3	3.47	
Internal POR threshold	Vth_POR	0.4		0.7	
Digital I/O pins[3)]					
For VDDIO, BT_VDDO = 1.8 V					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–		0.35 × VDDIO	
Output high voltage @ 2 mA	VOH	VDDIO – 0.40		–	
Output low voltage @ 2 mA	VOL	–		0.45	
RF switch control output pins[3)]					
For VDDIO_RFSW = 3.3 V					
Output high voltage @ 2 mA	VOH	VDDIO_RFSW – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–		0.4	
REG_ON Pins					
Input capacitance	CIN	_	_	5	pF
Input high voltage	VIH	1.2	_	VBAT	V
Input low voltage	VIL	_	_	0.3	V
Pull down resistance	R_{PD}	_	50	_	kΩ

1) CYW55912 is functional across this range of voltages. Optimal RF performance specified in the datasheet, however, is guaranteed only for 3.13 V < VBAT < 3.6 V.

2) The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed.
Voltage transients as high as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.

3) Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

7.4. Electrostatic Discharge (ESD) specification

Extreme caution must be exercised to prevent electrostatic discharge damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

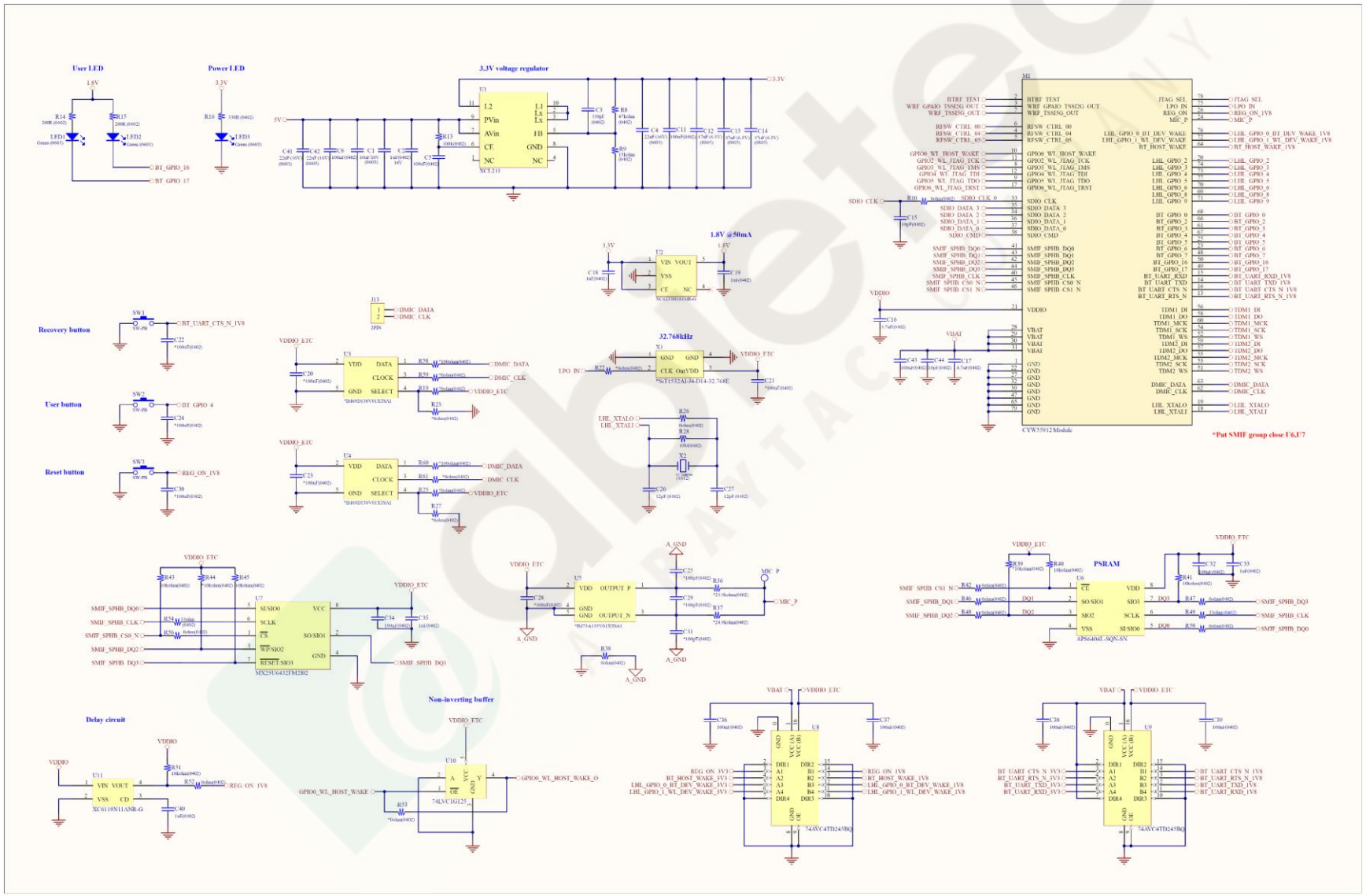
Table 6 ESD specifications

Pin type	Symbol	Conditions	ESD rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/ JESD22-A114	+/- 2	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	+/- 250	V
Latch-up	_	At 125°C	+/- 200	mA

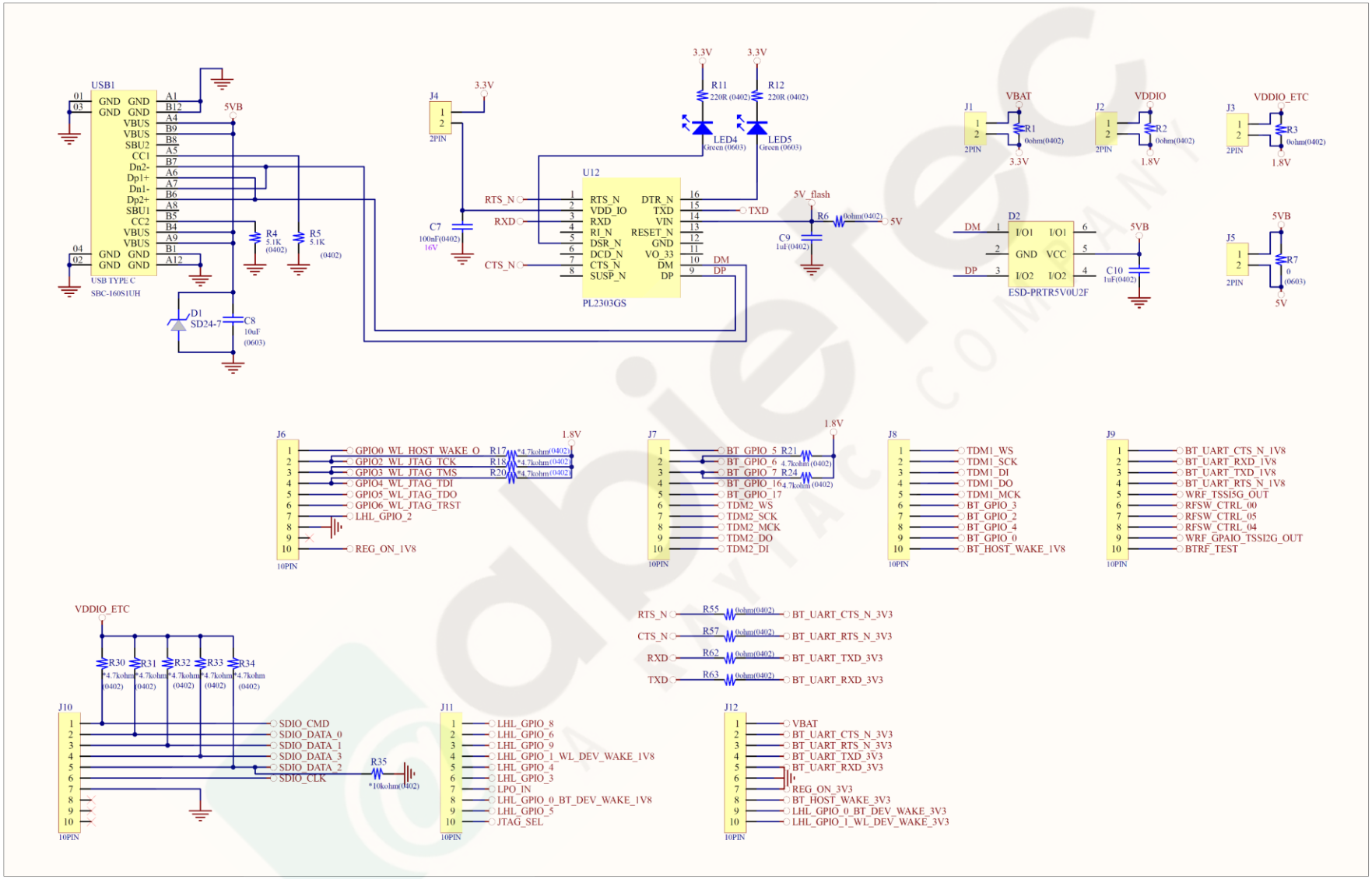
8. Reference circuit

- AI55912-P / AI55912-U module

AI55912-DB (P/U) page1-1



AI55912-DB (P/U) page1-2



9. Notes and cautions

Modules are not designed to last for a lifetime. Like general products, it is expected to wear out after continuous usage over the years. To assure that the product will perform better and last longer, please make sure you:

A. Follow the guidelines of this document while designing the circuit/end-product. Any discrepancy in core Wi-Fi technology and technical specification of IC should refer to the definition of Wi-Fi Organization and Infineon Technologies as the final reference.

B. Do not supply voltage that is not within the range of the specification.

C. Eliminate static electricity at any cost when working with the module, as it may cause damage. It is highly recommended to add anti-ESD components to circuit design to prevent damage from real-life ESD events. Anti-ESD methods can also be applied in mechanical design.

D. Do not expose modules to direct sunlight for long durations. Modules should be kept away from humid and salty air conditions and any corrosive gases or substances. Store it within -40℃ to +125℃ before and after installation.

E. Avoid any physical shock or intense stress to the module or its surface.

F. Do not wash the module. No-Clean Paste is used in production. Washing it will oxidize the metal shield and have a chemical reaction with No-Clean Paste. Functions of the module are not guaranteed if it has been cleaned.

The module is not suitable for a life support device or system and is not allowed to be used in destructive devices or systems in any direct or indirect way. The customer agrees to indemnify abietec for any losses when applying modules in applications such as the ones described above.

10. Useful links

Official page of CYW55912: https://www.infineon.com/part/CYW55912
A brief introduction to CYW55912

Development Environment/Tool: **ModusToolbox™ Software**

Infineon AIROC™ connected MCU: https://www.infineon.com/products/wireless-connectivity/airoc-connected-mcu. All the necessary technical files and information about Infineon's chip are on this website.

Infineon all Forums: https://community.infineon.com/t5/Forums/ct-p/products/page/1
A highly recommended website for firmware developers. Interact, discuss, and consult with other fellow developers and Infineon's employees to get answers to your questions. The site also includes detailed tutorials to help you get started.

Full list of abietec's(Raytac group) Wi-Fi modules

- **AN7002Q series (QFN package IC)**

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	Size	Weight
AN7002Q	nRF7002	AN7002Q	1	Chip Antenna	17.1 x 10.8 x 2.1 mm	0.78 (±0.02g)
		AN7002Q-P	1	PCB Antenna	17.1 x 10.8 x 2.1 mm	0.79 (±0.02g)
		AN7002Q-U	1	u.FL Connector	16.4 x 10.8 x 2.1 mm	0.85 (±0.02g)

Full list of abietec's(Raytac group) Bluetooth modules

AN54LQ series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	NVM
AN54LQ	nRF54L15	AN54LQ-15	1	Chip Antenna	256 kB	1.5 MB
	nRF54L10	AN54LQ-10	1		192 kB	1MB
	nRF54L05	AN54LQ-05	1		96 kB	0.5MB
AN54LQ-P	nRF54L15	AN54LQ-P15	1	PCB Antenna	256 kB	1.5 MB
	nRF54L10	AN54LQ-P10	1		192 kB	1MB
	nRF54L05	AN54LQ-P05	1		96 kB	0.5MB
AN54LQ-U	nRF54L15	AN54LQ-U15	1	u.FL Connector	256 kB	1.5 MB
	nRF54L10	AN54LQ-U10	1		192 kB	1MB
	nRF54L05	AN54LQ-U05	1		96 kB	0.5MB

AN54LV series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	NVM
AN54LV	nRF54L15	AN54LV-15	1	Chip Antenna	256 kB	1.5 MB
AN54LV-P		AN54LV-P15	1	PCB Antenna		

MDBT53 series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT53	nRF5340	MDBT53-1M	1	Chip Antenna	512 kB	1 MB
MDBT53-P	nRF5340	MDBT53-P1M	1	PCB Antenna	512 kB	1 MB
MDBT53-U	nRF5340	MDBT53-U1M	1	u.FL Connector	512 kB	1 MB

MDBT53V series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT53V	nRF5340	MDBT53V-1M	1	Chip Antenna	512 kB	1 MB
MDBT53V-P	nRF5340	MDBT53V-P1M	1	PCB Antenna	512 kB	1 MB

MDBT50 series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT50	nRF52820	MDBT50-256R	1	Chip Antenna	32 kB	256 kB
	nRF52833	MDBT50-512K	1		128 kB	512 kB
MDBT50-P	nRF52820	MDBT50-P256R	1	PCB Antenna	32 kB	256 kB
	nRF52833	MDBT50-P512K	1		128 kB	512 kB

MDBT50Q series (aQFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT50Q	nRF52840	MDBT50Q-1MEN	3	Chip Antenna	256 kB	1 MB
	nRF52840	MDBT50Q-1MV2	2			
	nRF52833	MDBT50Q-512K	1		128 kB	512 kB
MDBT50Q-P	nRF52840	MDBT50Q-P1MEN	3	PCB Antenna	256 kB	1 MB
	nRF52840	MDBT50Q-P1MV2	2			
	nRF52833	MDBT50Q-P512K	1		128 kB	512 kB
MDBT50Q-U	nRF52840	MDBT50Q-U1MEN	3	u.FL Connector	256 kB	1 MB
	nRF52840	MDBT50Q-U1MV2	2			
	nRF52833	MDBT50Q-U512K	1		128 kB	512 kB
Dongle	nRF52840	MDBT50Q-RX	1, 2	PCB Antenna	256 kB	1 MB
		MDBT50Q-CX-40	1			
	nRF52833	MDBT50Q-CX-33	1		128 kB	512 kB

MDBT42T series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42T	nRF52805	MDBT42T-192K	1	Chip Antenna	24 kB	192 kB
MDBT42T-P		MDBT42T-P192K		PCB Antenna		

MDBT42TV series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42TV	nRF52805	MDBT42TV-192K	1	Chip Antenna	24 kB	192 kB
MDBT42TV-P		MDBT42TV-P192K		PCB Antenna		

MDBT42 series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42	nRF52832	MDBT42-512KV2	2	Chip Antenna	64 kB	512 kB
MDBT42-P		MDBT42-P512KV2		PCB Antenna		

MDBT42V series (WLCSP package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42V	nRF52832	MDBT42V-512KV2	2	Chip Antenna	64 kB	512 kB
MDBT42V-P		MDBT42V-P512KV2		PCB Antenna		

MDBT42Q series (QFN package IC)

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT42Q	nRF52832	MDBT42Q-512KEN	3	Chip Antenna	64 kB	512 kB
	nRF52832	MDBT42Q-512KV2	2			
	nRF52810	MDBT42Q-192KV2	2		24 kB	192 kB
	nRF52811	MDBT42Q-192KL	1			
MDBT42Q-P	nRF52832	MDBT42Q-P512KEN	3	PCB Antenna	64 kB	512 kB
	nRF52832	MDBT42Q-P512KV2	2			
	nRF52810	MDBT42Q-P192KV2	2		24 kB	192 kB
	nRF52811	MDBT42Q-P192KL	1			
MDBT42Q-U	nRF52832	MDBT42Q-U512KEN	3	u.FL Connector	64 kB	512 kB
	nRF52832	MDBT42Q-U512KV2	2			

MDBT40 series

Series	Nordic Solution	Raytac No.	IC Ver.	Antenna	RAM	Flash Memory
MDBT40	nRF51822	MDBT40-256V3	3	Chip Antenna	16 kB	256 kB
		MDBT40-256RV3			32 kB	256 kB
MDBT40-P	nRF51822	MDBT40-P256V3	3	PCB Antenna	16 kB	256 kB
		MDBT40-P256RV3			32 kB	256 kB

Release Note

- 2025/08/28 Version 0.1: Preliminary.